Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A circuit device manufacturing method comprising:

preparing a conductive foil;

providing in the conductive foil, isolation trenches having a depth less than a thickness of the conductive foil;

providing a conductive plating layer on the conduction foil between the isolation trenches, said conductive plating layer being recessed from edges of the conduction foil;

providing circuit elements on the conductive plating layer;

providing an insulating resin to cover collectively the circuit elements and to fill the isolation trenches;

~~forming~~ exposing conducive patterns by removing the conductive foil from opposite to the side where the circuit elements are provided until the insulating resin in the trenches is exposed; and

dicing the insulating resin appropriately to separate the circuit elements.

2. (Previously presented) The circuit device manufacturing method according to claim 1, further comprising:

electrically connecting electrodes of the circuit elements to the conductive foil before providing the insulating resin.

3. (Original) The circuit device manufacturing method according to claim 1, wherein the conductive foil is formed of any one of copper, aluminum, and iron-nickel.

4. (Previously presented) The circuit device manufacturing method according to claim 1, wherein the conductive plating layer partially covers the conductive foil.

5. (Original) The circuit device manufacturing method according to claim 4, wherein the conductive plating layer is formed by gold or silver plating.

6. (Original) The circuit device manufacturing method according to claim 1, wherein the isolation trenches formed selectively on the conductive foil are formed by chemical or physical etching.

7. (Original) The circuit device manufacturing method according to claim 1, wherein at least one of bare semiconductor chips and chip circuit components are fixed as the circuit elements.

8. (Original) The circuit device manufacturing method according to claim 2, wherein the connecting member is formed by wire bonding.

9. (Previously presented) The circuit device manufacturing method according to claim 8, wherein the wire bonding is applied onto the conductive plating layer.

10. (Previously presented) The circuit device manufacturing method according to claim 8, wherein a position of the wire bonding is determined by contrasting between a region of the conductive foil without the conductive plating and a region of the conductive plating layer on the conductive foil.

11. (Previously presented) The circuit device manufacturing method according to claim 1, wherein the insulating resin is provided by transfer molding.

12. (Previously presented) The circuit device manufacturing method according to claim 1, wherein

the circuit elements are provided in blocks which are aligned in matrix fashion on the conductive foil.

13. (Previously presented) The circuit device manufacturing method according to claim 12, wherein the insulating resin is provided by transfer molding for every block.

14. (Previously presented) The circuit device manufacturing method according to claim 12, wherein the insulating resin is diced to separate the blocks.

15. (Previously presented) The circuit device manufacturing method according to claim 14, wherein the dicing is carried out by using alignment marks provided at a periphery of each block.

16. (Previously presented) The circuit device manufacturing method according to claim 14, wherein the dicing is carried out by using opposing alignment marks provided at a periphery of each block.

17. (Previously presented) A circuit device manufacturing method according to claim 1, further comprising:

after providing the trenches in the conductive foil, covering the conductive foil including surfaces of the isolation trenches with a resist layer.

18. (Previously presented) A circuit device manufacturing method according to claim 17, further comprising:

after covering the conductive foil with the resist layer, selectively removing the resist layer on the conductive foil.

19. (Previously presented) A circuit device manufacturing method according to claim 18, further comprising:

providing the conductive plating layer where the resist layer has been selectively removed.

20. (New) The circuit device manufacturing method according to claim 1 wherein the dicing is carried out by using alignment marks provided at a periphery of each block.

21. (New) The circuit device manufacturing method according to claim 1 wherein the dicing is carried out by using opposing alignment marks provided at a periphery of each block.